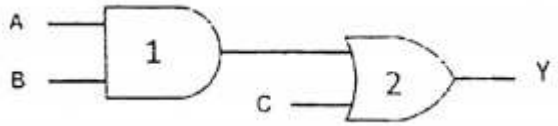
Model Question Paper I

ANALOG & DIGITAL CIRCUITS

Time: 3 Hour *Max.Marks: 75*

PART A

I. Answer **all** questions in one word or one sentence. Each question carries 1 mark.

1	Define class 'C' operation of power amplifier.	M1.01	R
2	Define Barkhausen's criterion for oscillations	M1.02	R
3	Define CMRR of an op-amp.	M2.01	R
4	List the applications of op amp circuits.	M2.03	R
5	Define De Morgan's theorem	M3.03	R
6	Identify the two gates represented by 1 and 2 in the figure below. Write the Boolean expression for the output Y 	M3.03	A
7	Illustrate the truth table of XOR gate	M3.02	U
8	Show the circuit symbol of SR flip flop	M4.02	R
9	List any two examples of sequential logic circuits	M4.03	R

PART B

II. Answer any **eight** questions from the following, each question carries 3 marks.

1	List the classifications of power amplifiers based on the period of conduction.	M1.01	R
2	Explain positive feedback and negative feedback	M1.02	U

3	List advantages of crystal oscillators.	M1.03	R
4	Compare astable and bistable multi vibrators	M1.04	U
5	Explain non inverting amplifiers using op amp	M2.02	U
6	How does an op amp work as a comparator?	M2.04	R
7	List characteristics of an ideal op-amp.	M2.01	R
8	Explain a typical op-amp stage with the help of its block diagram	M2.01	U
9	Convert the hex number $(F8E6.39)_{16}$ to decimal number.	M3.01	A
10	List out different modes of operations of shift registers	M4.03	R

PART C

Answer ALL questions. Each question carries 7 marks.

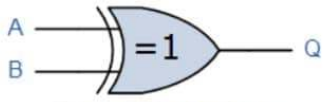
III	Describe the working principle of RC phase shift oscillator with a neat diagram	M1.03	R
	OR		
IV	Explain the operation of astable multivibrator with a neat diagram	M1.04	U
V	Describe the role of op amp in the working of half wave precision rectifiers.	M2.03	R
	OR		
VI	Obtain an expression for output voltage of an inverting amplifier	M2.03	U
VII	Minimize the following boolean function F(A, B, C, D) = Σm(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)	M3.03	A
	OR		
VIII	Explain 1's complement addition and subtraction using suitable example	M3.03	U
IX	Simplify the following Boolean expression using K map $Y = \overline{A}.\ \overline{B}.\ C + \overline{A}.\ \overline{B}.\ \overline{C} + \overline{A}.\ \overline{B}.\ C + A.\ B.\ C$	M3.03	A
	OR		
X	Explain 2's complement addition and subtraction using suitable example	M3.03	U

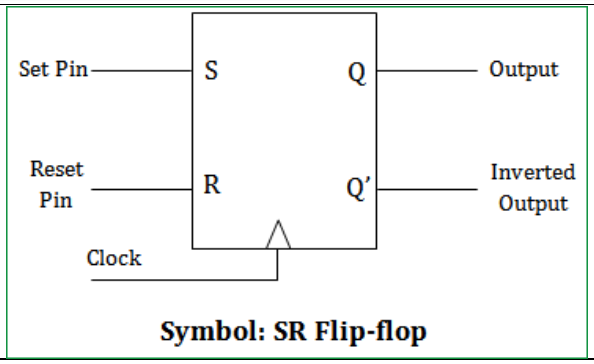
XI	Differentiate between SR and JK flip flops	M4.03	U
	OR		
XII	With neat diagram, explain the operation of R-2R ladder type DAC	M4.03	U
XIII	Explain the implementation of full adder using half adder	M4.03	U
	OR		
XIV	Construct a mod 8 asynchronous counter. Also draw its logic, timing diagram and truth table.	M4.03	A

Scoring Indicators

Model Question Paper I

Analog & Digital Circuits

<table>
<tr><th>Q No</th><th>Scoring Indicators</th><th>Split score</th><th>Sub Total</th><th>Total Score</th></tr>
<tr><td></td><td>PART A</td><td></td><td></td><td></td></tr>
<tr><td>I. 1</td><td>When the collector current flows for less than half cycle of the input signal, the power amplifier is known as class C power amplifier.</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I. 2</td><td>| β A | = 1
□ β A = 2 π n, n □ 0, 1, 2,…</td><td>0.5
0.5</td><td>1</td><td>1</td></tr>
<tr><td>I. 3</td><td>The ratio of the common-mode gain to differential-mode gain.</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I. 4</td><td>Write any two application(summing amplifier, inverting amplifier, comparator etc)</td><td>0.5
0.5</td><td>1</td><td>1</td></tr>
<tr><td>I. 5</td><td>$\overline{A \cdot B} \equiv \overline{A} + \overline{B}$
and
$\overline{A + B} \equiv \overline{A} \cdot \overline{B}$,</td><td>0.5
0.5</td><td>1</td><td>1</td></tr>
<tr><td>I. 6</td><td>AND,OR
Y=AB+C</td><td>0.5
0.5</td><td>1</td><td>1</td></tr>
<tr><td>I. 7</td><td>Symbol
 

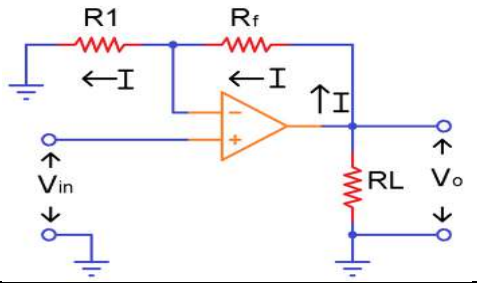
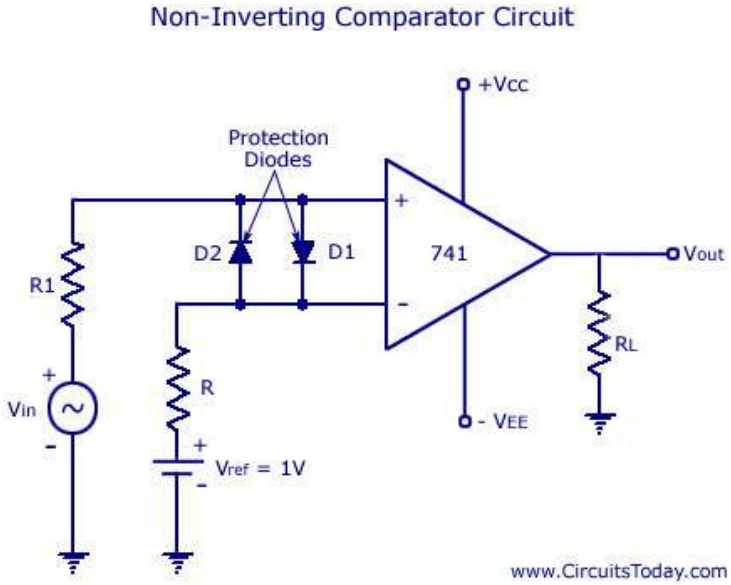
2-input Ex-OR Gate
Truth Table
A B Q
0 0 0
0 1 1
1 0 1
1 1 0
Boolean Expression Q = A XOR B</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>I. 8</td><td> 

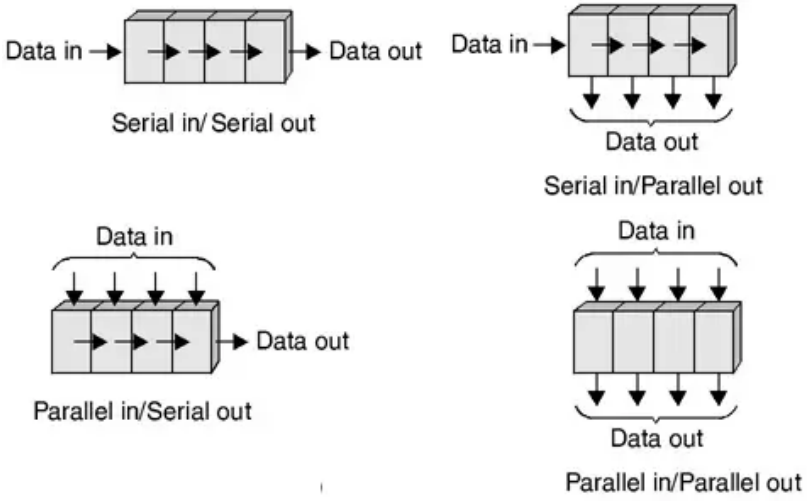
Symbol: SR Flip-flop</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
</table>

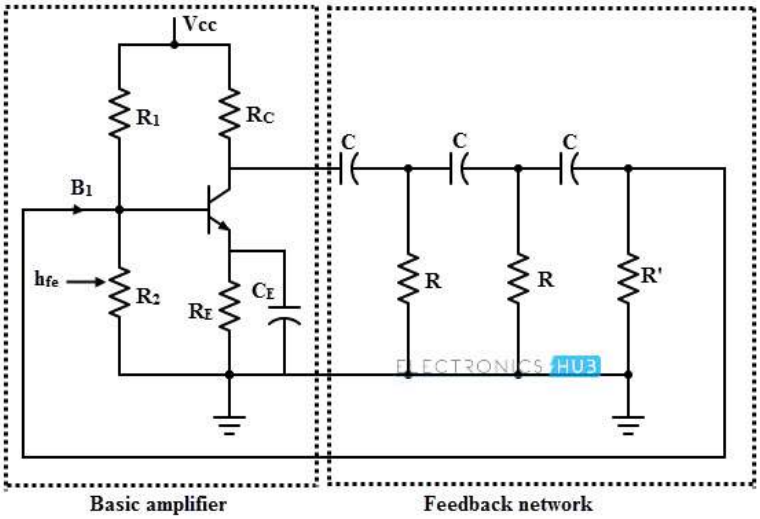
<table>
<tr><td>I. 9</td><td>Flip-flop, register, counter …. Write any two</td><td>0.5
0.5</td><td>1</td><td>1</td></tr>
<tr><td></td><td>PART B</td><td></td><td></td><td></td></tr>
<tr><td>II. 1</td><td>Class A:This single output transistor is biased around the Q-point within the middle of its load line and so is never driven into its cut-off or saturation regions thus allowing it to conduct current over the full 360 degrees of the input cycle.
ClassB:Transistor device of the class B amplifier only conducts through one half or 180 degrees of the output.
Class C:The conduction angle for the transistor is significantly less than 180 degrees, and is generally around the 90 degrees area.</td><td>1

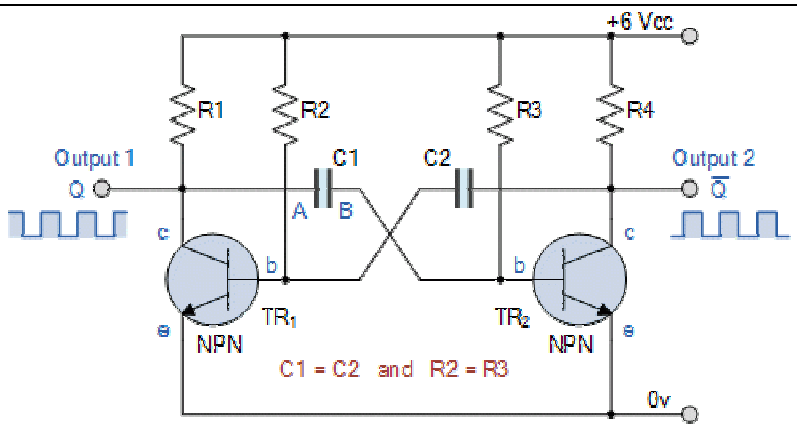
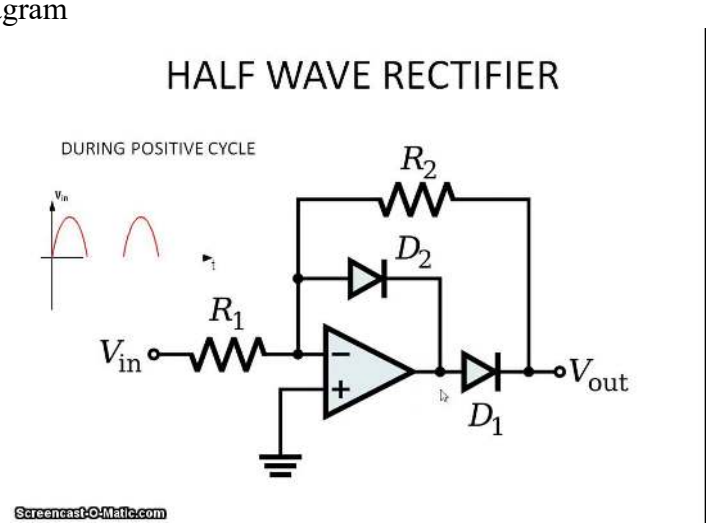
1

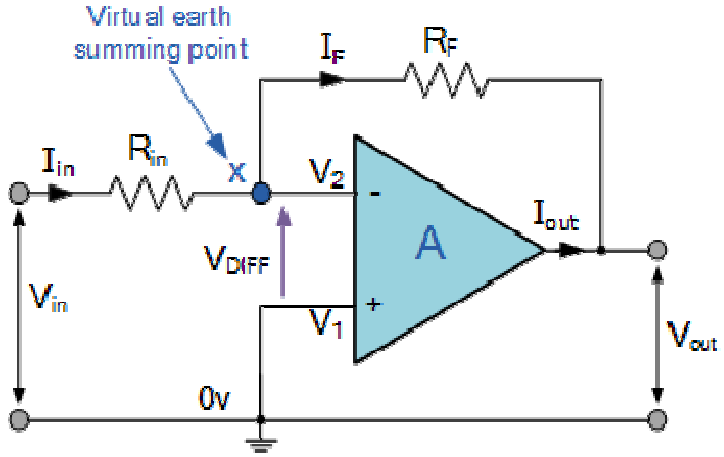
1</td><td>3</td><td>3</td></tr>
<tr><td>II. 2</td><td>Any three points , each carry one mark<table><tr><th>Positive</th><th>Negative</th></tr><tr><td>Input signal and output signal are in the same phase.</td><td>Weakens the input signal</td></tr><tr><td>Makes the input signal stronger.</td><td>Smaller than the gain of the system</td></tr><tr><td>Decreases the stability of the system.</td><td>Increases the stability of the state</td></tr></table></td><td>1
1
1</td><td>3</td><td>3</td></tr>
<tr><td>II. 3</td><td>Answer any three
● Higher stability
● High Q.
● Frequency Customization and Range is higher
● Low Phase Noise.</td><td>1
1
1</td><td>3</td><td>3</td></tr>
<tr><td>II. 4</td><td>Answer any three points<table><tr><th>Astable</th><th>Bistable</th></tr><tr><td>No stable state</td><td>Two stable state</td></tr><tr><td>No trigger needed</td><td>Trigger needed</td></tr><tr><td>Used as pulse generators</td><td>Used as flip flops</td></tr></table></td><td>1
1
1</td><td>3</td><td>3</td></tr>
</table>

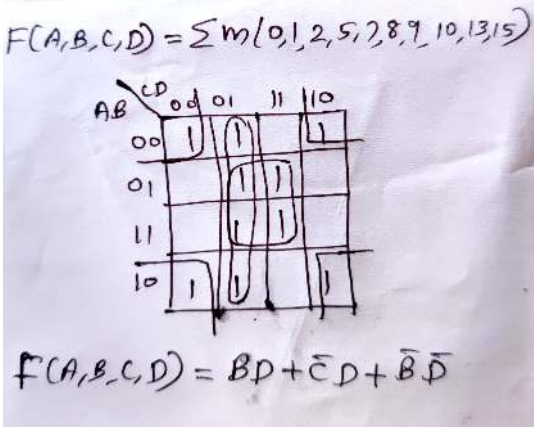
II. 5	**Diagram** **Explanation** In Non Inverting Operational Amplifiers, the input is fed to the non-inverting terminal and the output is in phase with the input. Closed loop gain = $1 + \frac{R_f}{R_1}$  	2 1	3	3
II. 6	**Diagram** **Explanation** The Op-amp comparator compares one analogue voltage level with another analogue voltage level, or some preset reference voltage, VREF and produces an output signal based on this voltage comparison. In other words, the op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two.  	2 1	3	3
II. 7	**Answer any three points** • Infinite open-loop gain G = v_{out} / v. ... • Infinite input impedance R_{in}, • Zero input offset voltage.	1 1 1	3	3

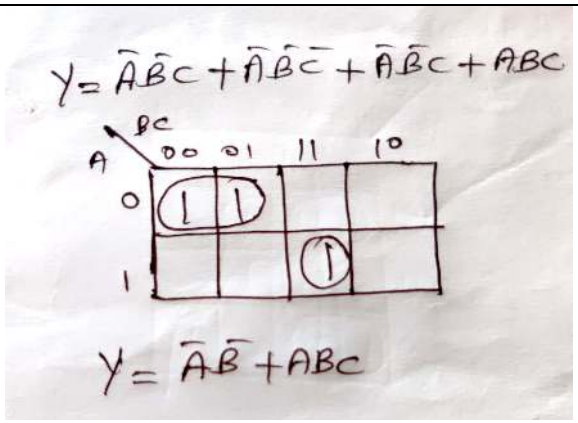
	● Infinite output voltage range. ● Infinite bandwidth with zero phase shift and infinite slew rate. ● Zero output impedance R.			
II. 8		3	3	3
II. 9	Steps Final answer $(F8E6.39)_{16} = (15 \times 16^3) + (8 \times 16^2) + (14 \times 16^1) + (6 \times 16^0) + (3 \times 16^{-1}) + (9 \times 16^{-2}) = (63718.22265625)_{10}$	2 1	3	3
II.10	**Answer any three(SISO,SIPO,PISO,PIPO)**  **Serial-in to Parallel-out (SIPO)** - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form. **Serial-in to Serial-out (SISO)** - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control. **Parallel-in to Serial-out (PISO)** - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control. **Parallel-in to Parallel-out (PIPO)** - the parallel data is loaded simultaneously into the register, and transferred	1 1 1	3	3

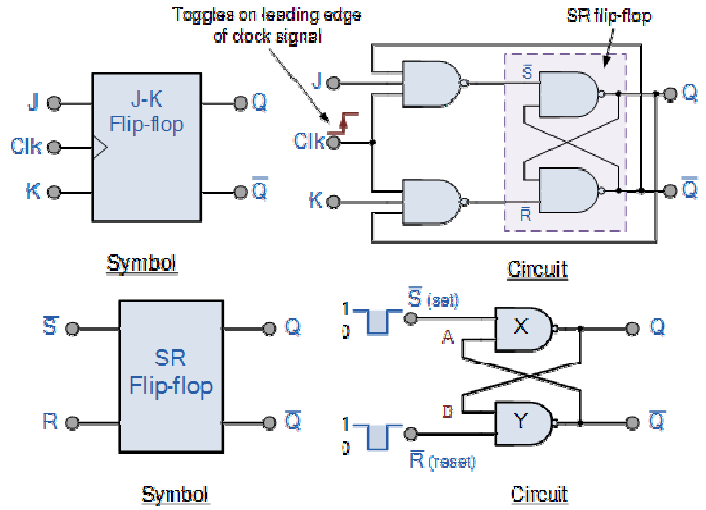
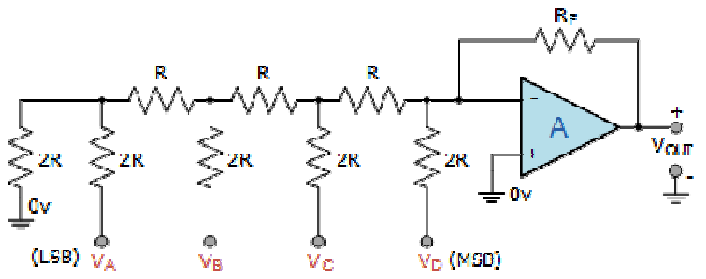
	together to their respective outputs by the same clock pulse.			
	PART C			
III	**Explanation** The basic RC Oscillator which is also known as a Phase-shift Oscillator, produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor (RC) ladder network. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tank circuit). This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360 degree. By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3-ganged variable capacitor because capacitive reactance (XC) changes with a change in frequency as capacitors are frequency-sensitive components. However, it may be required to re-adjust the voltage gain of the amplifier for the new frequency. **Diagram**  	4 3	7	7
IV	**Diagram**	4	7	7

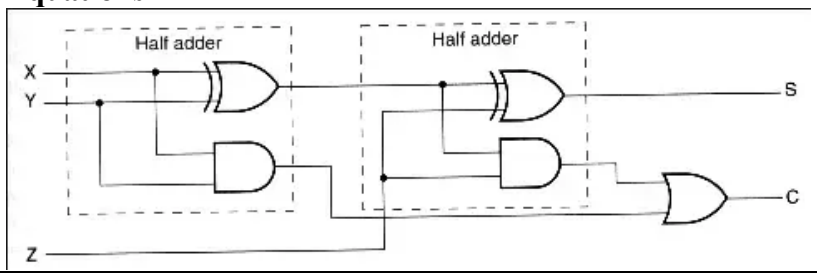
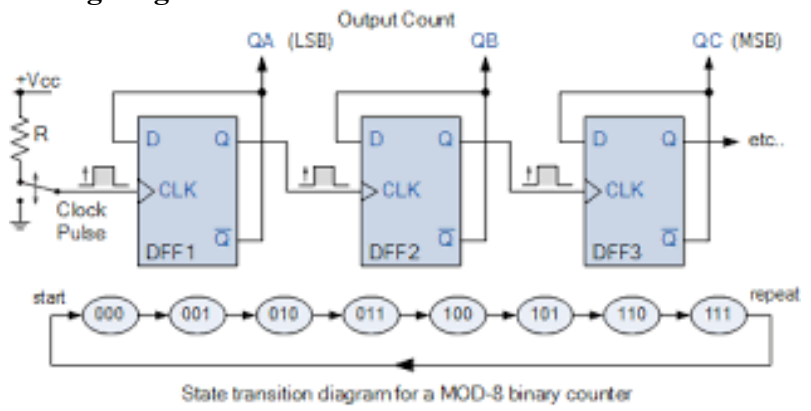
	 It is implemented by the coupling capacitors that instantly transfer voltage changes because the voltage across a capacitor cannot suddenly change. In each state, one transistor is switched on and the other is switched off. Accordingly, one fully charged capacitor discharges (reverse charges) slowly thus converting the time into an exponentially changing voltage. At the same time, the other empty capacitor quickly charges thus restoring its charge (the first capacitor acts as a time-setting capacitor and the second prepares to play this role in the next state). The circuit operation is based on the fact that the forward-biased base-emitter junction of the switched-on bipolar transistor can provide a path for the capacitor restoration.	3		
V	Diagram  The precision rectifier is another rectifier that converts AC to DC, but in a precision rectifier we use an op-amp to compensate for the voltage drop across the diode, that is why we are not losing the 0.6V or 0.7V voltage drop across the diode, also the circuit can be constructed to have some gain at the output of the amplifier as well. In this case, when the input is greater than zero, D1 is off, and D2 is on, so the output is zero because the other end of	4 3	7	7

	R2 is connected to the virtual ground and there is no current through R2. When the input is less than zero, D1 is on, and D2 is off, so the output is like the input with an amplification of -R2/R1			
VI	Diagram  $i = \frac{Vin - Vout}{Rin + Rf}$ $\text{therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$ $i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$ $\text{so } \frac{Vin}{Rin} - V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$ $\text{and as, } i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf} \qquad \frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$ $\text{the Closed Loop Gain (Av) is given as, } \frac{Vout}{Vin} = -\frac{Rf}{Rin}$	4 3	7	7

VII	 K map Steps Final result *(other variations in answer may accept)*	4 2 1	7	7
VIII	Addition (Any Example) Add 1101 +(-1001) 1. First, find the 1's complement of the negative number 1001. So, for finding 1's complement, change all 0 to 1 and all 1 to 0. The 1's complement of the number 1001 is 0110. 2. Now, add both the numbers, i.e., 1101 and 0110; 1101+0110=1 0011 3. By adding both numbers, we get the end-around carry 1. We add this end around carry to the LSB of 0011. 0011+1=0100 Subtraction (Any Example) Subtracting 10101 - 00111 1. Take 1's complement of subtrahend 00111, which comes out 11000. 2. Take sum them, 10101+11000 =1 01101. 3. In the above result, we get the carry bit 1, so add this to the LSB of a given result, i.e., 01101+1=01110,	3.5 3.5	7	7
IX	K map	4 2 1	7	7

	 Steps Final result			
X	Addition (Student can choose any two binary numbers for example) 1101 + -1001 1. Find the 2's complement of the negative number 1001. So, for finding 2's complement, change all 0 to 1 and all 1 to 0 or find the 1's complement of the number 1001. The 1's complement of the number 1001 is 0110, and add 1 to the LSB of the result 0110. So the 2's complement of number 1001 is 0110+1=0111 2. Add both the numbers, i.e., 1101 and 0111; 1101+0111=1 0100 3. By adding both numbers, we get the end-around carry 1. We discard the end-around carry. So, the addition of both numbers is 0100. Subtraction (Student can choose any two binary numbers for example) 10101- 00111 1. Take 2's complement of subtrahend 00111, which is 11001. Take Sum 10101+11001 =1 01110. 2. In the above result, we get the carry bit 1. So we discard this carry bit and remaining is the final result	3.5 3.5	7	7

	and a positive number.			
XI	**Diagram** **Explanation**  Symbol Circuit The **SR flip-flop**, also known as a *SR Latch*, can be considered as one of the most basic sequential logic circuits possible. This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which will "SET" the device (meaning the output = "1"), and is labelled **S** and one which will "RESET" the device (meaning the output = "0"), labelled **R**. The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle".	4 3	7	7
XII	**Diagram**  As its name implies, the "ladder" description comes from the ladder-like configuration of the resistors used within the network. A R-2R resistive ladder network provides a simple means of converting digital voltage	4	7	7

	signals into an equivalent analogue output. Input voltages are applied to the ladder network at various points along its length and the more input points the better the resolution of the R-2R ladder. The output signal as a result of all these input voltage points is taken from the end of the ladder which is used to drive the inverting input of an operational amplifier	3		
XIII	**Diagram** **Equations** 	4 3	7	7
XIV	**Truth table** **Circuit diagram** **logic diagram** **Timing diagram** 	2 3 1 1	7	7

Module wise question analysis

Question No	Module	No of questions

	I	II	III	IV	
Part A (1 Mark)	2	2	3	2	9
Part B (3 Marks)	4	4	1	1	10
Part C (7 Marks)	2	2	4	4	12
Total questions	**8**	**8**	**8**	**7**	**31**
Total (Marks)-123	**28**	**28**	**34**	**33**	

Cognitive level wise question analysis

Question No	**Cognitive level**			**No of questions**
	Remember	**Understand**	**Apply**	
Part A (1 Mark)	7	1	1	9
Part B (3 Marks)	5	4	1	10
Part C (7 Marks)	2	7	3	12
Total questions	**14**	**12**	**5**	**31**
Total (Marks)=123	**36**	**62**	**25**	

Prepared By :	Scrutinised By :
	
Nikhil V T Lecturer Govt Polytechnic College, Kannur	Shithin P V Lecturer Govt. Polytechnic College, Kannur

Model Question Paper II

ANALOG & DIGITAL CIRCUITS

Time: 3 Hour *Max.Marks: 75*

PART A

I. Answer **all** questions in one word or one sentence. Each question carries 1 mark.

1	Define the term feedback in an amplifier.	M 1.02	R
2	List the conditions for sustained oscillations	M 1.02	R
3	Define voltage gain of an op-amp.	M 2.01	R
4	List the applications of op amp circuits?	M 2.03	R
5	List two laws associated with Boolean algebra	M 3.03	R
6	Differentiate SOP and POS representation of Boolean expression.	M 3.04	U
7	Convert the decimal number $(17)_{10}$ to its binary equivalent number	M 3.01	A
8	Explain the term combinational circuit	M 4.01	R
9	List any two applications of flip flops	M 4.02	R

PART B

II. Answer any **eight** questions from the following, each question carries 3 marks.

1	Explain a complementary symmetry push pull amplifier?	M 1.01	R
2	Compare positive and negative feedback	M 1.02	U
3	List the classifications of multi vibrator circuits?	M 1.04	R
4	Compare class A and class B power amplifiers	M 1.01	U
5	Explain full wave precision rectifier with circuit diagram	M 2.04	U
6	Describe working principle of summing amplifier	M 2.03	R
7	List the characteristics of ideal op amp	M 2.01	R
8	Compare positive and negative level comparator with circuit diagrams	M 2.04	U
9	Convert the binary number $(11011.011)_2$ to decimal	M 3.01	A
10	Describe the working of multiplexer circuit with an example	M 4.01	R

PART C

Answer ALL questions. Each question carries 7 marks.

III	Describe the working principle of crystal oscillator with a neat diagram	M 1.03	R
	OR		
IV	Explain the operation of bistable multivibrator with a neat diagram	M 1.04	U
V	Explain op amp as inverting amplifier. Derive its output voltage	M 2.02	U
	OR		
VI	Show the concept of virtual ground with the help of a neat diagram	M 2.01	R
VII	Apply Demorgan's theorem and simplify the following expression $\overline{(A\bar{B} + \bar{C}D + EF)}$	M 3.03	A
	OR		
VIII	Explain about common logic gates and universal gates in digital circuits	M 3.02	U
IX	Using K map,minimize the following boolean function f(A, B, C, D) = Σm(1, 2, 4, 5, 7, 8, 9, 10, 13, 15)	M 3.04	A
	OR		
X	Explain 2's complement addition and subtraction using suitable example	M 3.01	U
XI	Explain the operation of R-2R ladder type DAC using neat diagram	M 4.04	U
	OR		
XII	Differentiate between SR and JK flip flops	M 4.02	U
XIII	Draw the diagram of ramp type ADC and explain it.	M 4.04	U
	OR		
XIV	Construct half adder and half subtractor using basic gates. Draw its truth table.	M 4.01	A

Scoring Indicators

Model Question Paper II

ANALOG & DIGITAL CIRCUITS

Q No	Scoring Indicators	Split score	Sub Total	Total score
	PART A			
I. 1	The process by which some part or fraction of output is combined with the input is known as **feedback**.	1	1	1
I. 2	$\lvert \beta A \rvert = 1$ $\angle \beta A = 2 \pi n, \quad n \in 0, 1, 2,\ldots$	0.5 0.5	1	1
I. 3	**Voltage gain** is defined as the ratio of the output **voltage** to the input **voltage** in dB	1	1	1
I. 4	Write any two application(summing amplifier, inverting amplifier, comparator etc)	0.5 0.5	1	1
I. 5	Commutative A+B=B+A Associative A+(B+C)=(A+B)+C	0.5 0.5	1	1
I. 6	Sum of Products (SOP): It is formed by adding (OR operation) the product terms. These product terms are also called 'min-terms'. Product of Sums (POS): It is formed by multiplying(AND operation) the sum terms. These sum terms are also called 'max-terms'.	0.5 0.5	1	1
I. 7	$(17)_{10}=(10001)_2$	1	1	1
I. 8	Combinatorial circuit is a type of digital circuit which is implemented by Boolean circuits, where the output is a pure function of the present input only.	1	1	1
I. 9	1) Counters 2) Registers	0.5 0.5	1	1
	PART B			
II. 1	Diagram	2	3	3

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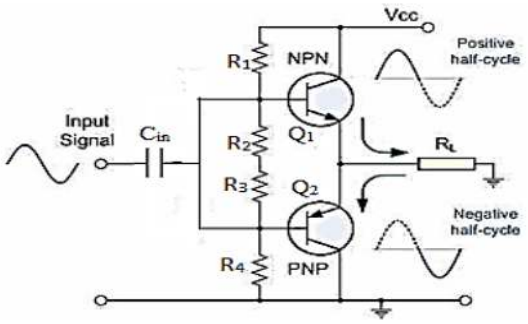
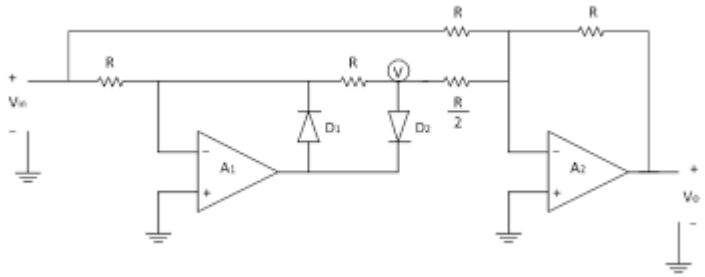
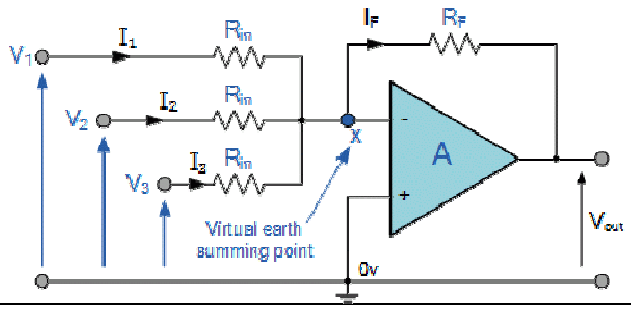
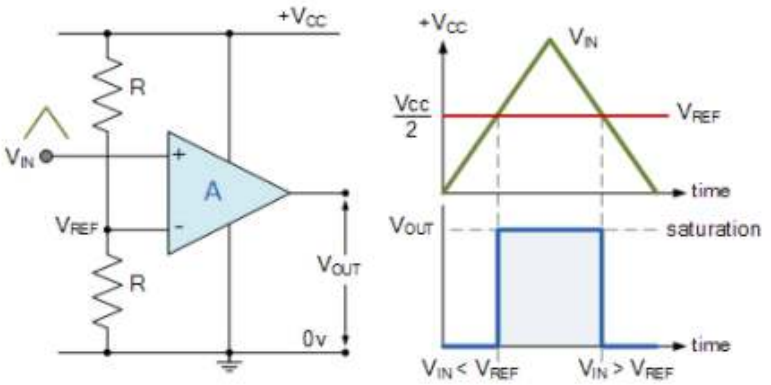
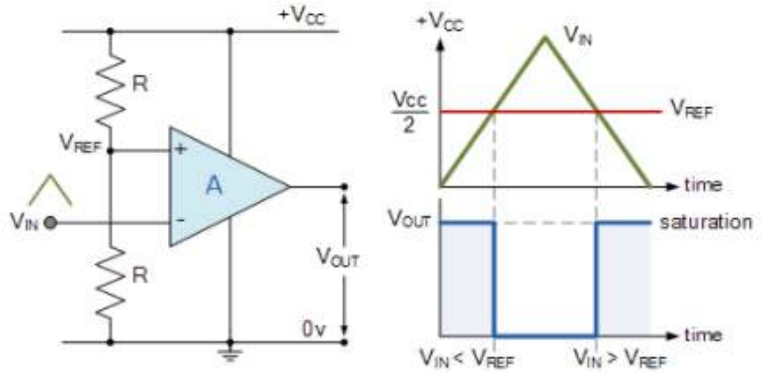
<tr>
<td></td>
<td> 

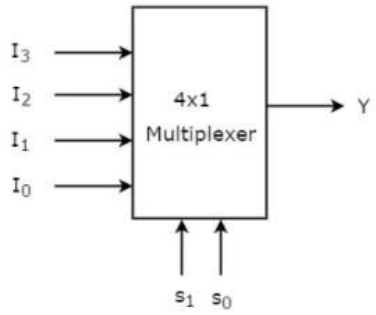
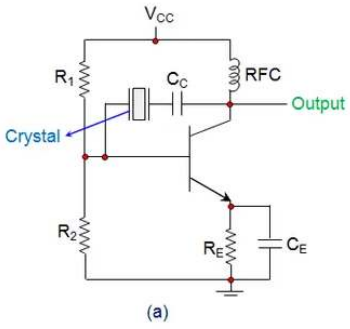
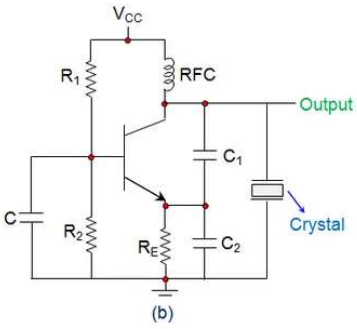
Explanation

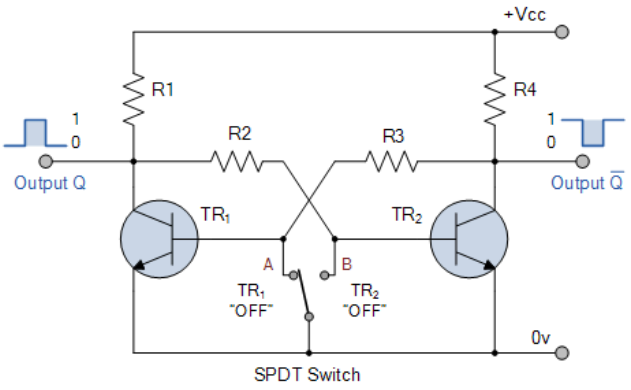
Arrangement uses two transistors having complementary symmetry
The resistors R1 and R2 provide the voltage divider bias to forward bias the Emitter-Base Junction of transistor Q1 and similarly Resistors R3 and R4 provide the voltage divider bias for Emitter-Base junction of transistor Q2

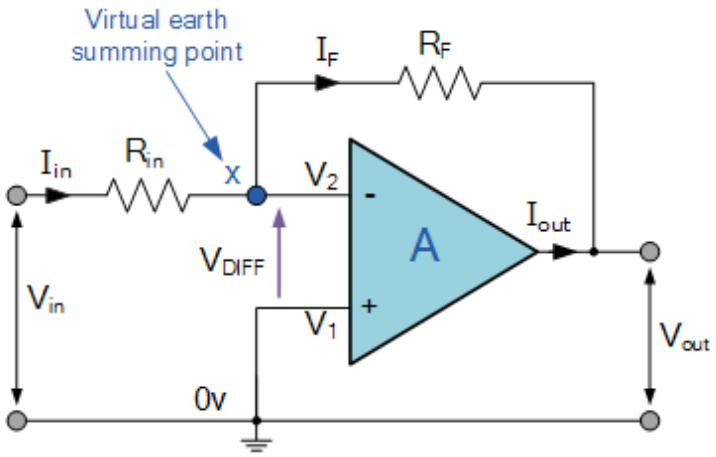
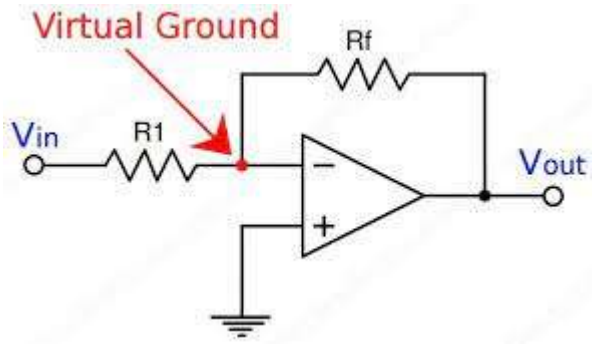
(Any two points)</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>II. 2</td>
<td>Any three points , each carry one mark
<table>
<tr><th>Positive</th><th>Negative</th></tr>
<tr><td>Input signal and output signal are in the same phase.</td><td>Weakens the input signal</td></tr>
<tr><td>Makes the input signal stronger.</td><td>Smaller than the gain of the system</td></tr>
<tr><td>Decreases the stability of the system.</td><td>Increases the stability of the state</td></tr>
</table></td>
<td>1
1
1</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>II. 3</td>
<td>Astable (Basic operation)
Bistable (Basic operation)
Monostable (Basic operation)</td>
<td>1
1
1</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>II. 4</td>
<td></td>
<td>3 x 1</td>
<td>3</td>
<td>3</td>
</tr>
</table>

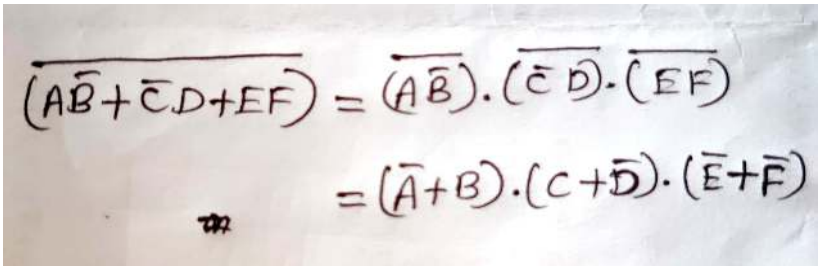
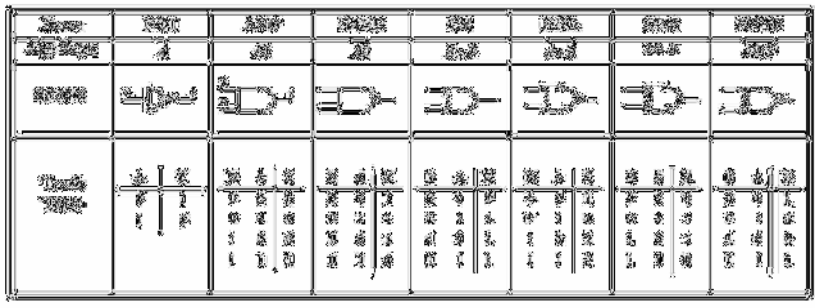
	<table><tr><th>Class A</th><th>Class B</th></tr><tr><td>In this P.A the operating point of RJT is at centre of load line.</td><td>In this P.A operating point of BJT is in cut off region.</td></tr><tr><td>Under no signal condition TX is ON</td><td>Under no signal condition TX is OFF</td></tr><tr><td>Conduction angle θ = 0° to 860°</td><td>Conduction angle θ = 0° to 180°</td></tr><tr><td>O/p signal is not distorted.</td><td>O/p is distorted i.e. o/p is just like rectified o/p.</td></tr><tr><td>η = 50%</td><td>η = 78.5%</td></tr></table> (Any three points)			
II. 5	Diagram  both the half cycles output is produced & in one direction only In positive half cycle Op-Amp A1 works as an inverting amplifier Op-amp A2 works as an inverting adder. In negative half cycle op-amp A1is zero. Op-amp A2 works as an inverting adder.	2 1	3	3
II. 6	Diagram Explanation 	2 1	3	3
II. 7	• Infinite open-loop gain • Infinite input impedance R_{in},	3*1	3	3

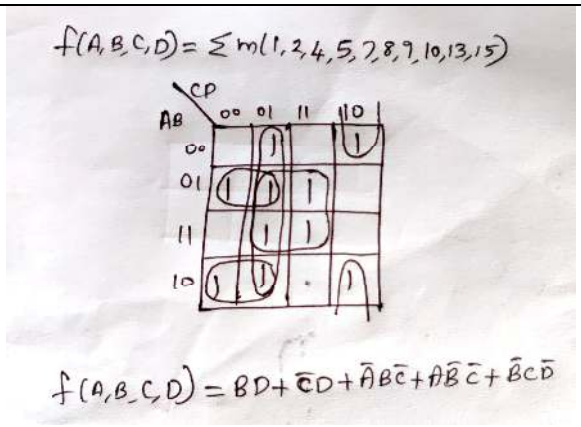
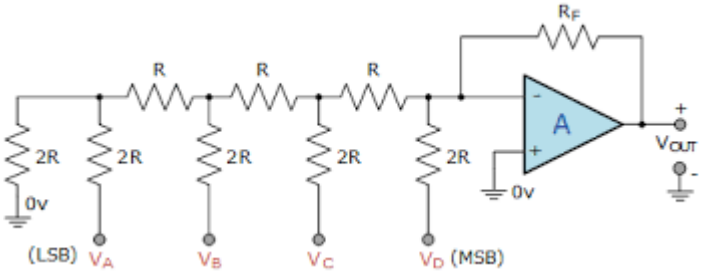
	● Zero input offset voltage. ● Infinite output voltage range. ● Infinite bandwidth with zero phase shift and infinite slew rate. ● Zero output impedance R. (Answer any three)			
II. 8	Positive Voltage Comparators  Negative Voltage Comparators  	1.5 1.5	3	3
II. 9	Steps Final answer $(11011.011)_2 = (1 \times 2^4) + (1 \times 2^3) + (0 \times 2^2) + (1 \times 2^1) + (1 \times 2^0) + (0 \times 2^{-1}) + (1 \times 2^{-2}) + (1 \times 2^{-3}) = (27.375)_{10}$	2 1	3	3
II.10		2	3	3

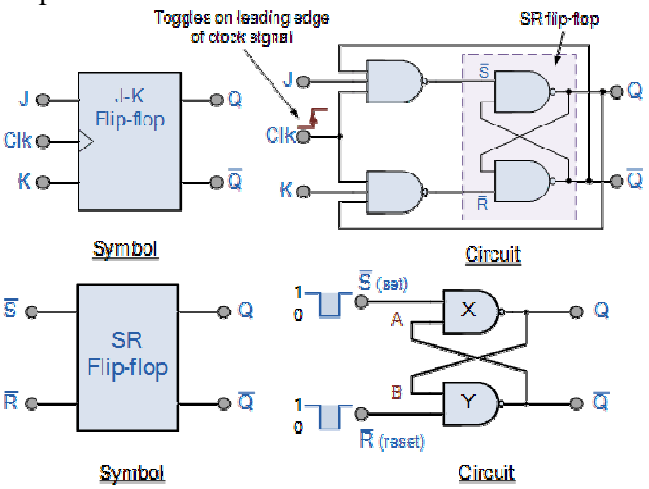
	4x1 Multiplexer 4x1 Multiplexer has four data inputs I_3, I_2, I_1 & I_0, two selection lines s_1 & s_0 and one output Y. The **block diagram** of 4x1 Multiplexer is shown in the following figure.  One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines. **Truth table** of 4x1 Multiplexer is shown below. **Selection Lines** | **Output** S_1 | S_0 | Y 0 | 0 | I_0 0 | 1 | I_1 1 | 0 | I_2 1 | 1 | I_3 From Truth table, we can directly write the **Boolean function** for output, Y as $$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$	1		
	PART C			
III	 (a)  (b) In the circuits shown, the resistors R1 and R2 form the voltage divider network while the emitter resistor RE stabilizes the circuit. Further, CE (Figure a) acts as an AC bypass capacitor while the coupling capacitor CC (Figure a) is used to block DC signal propagation between the collector and the base terminals. Next, the capacitors C1 and C2 form the capacitive voltage divider network in the case of Figure b. In addition, there is also a Radio Frequency Coil (RFC) in the circuits (both in Figure a and b) which offers dual advantage as it provides even the DC bias as well as frees the circuit-output from being affected by the AC signal on the power lines.	4 3	7	7

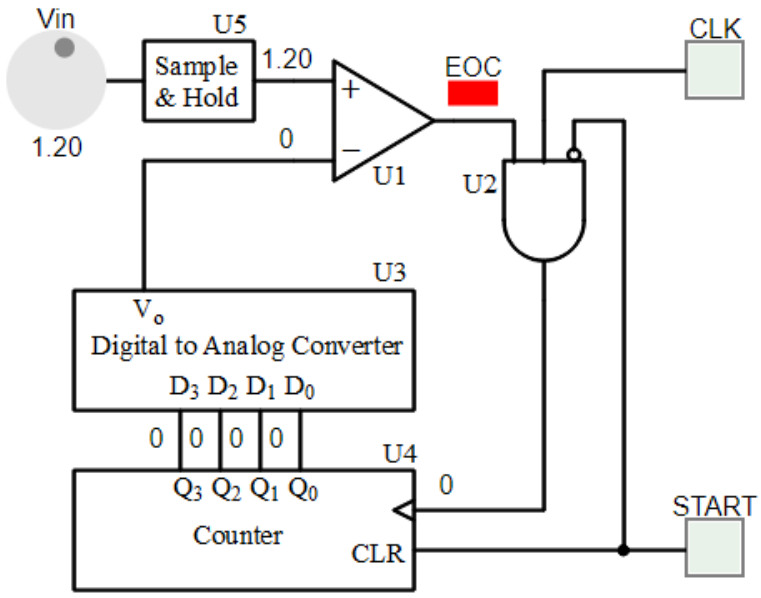
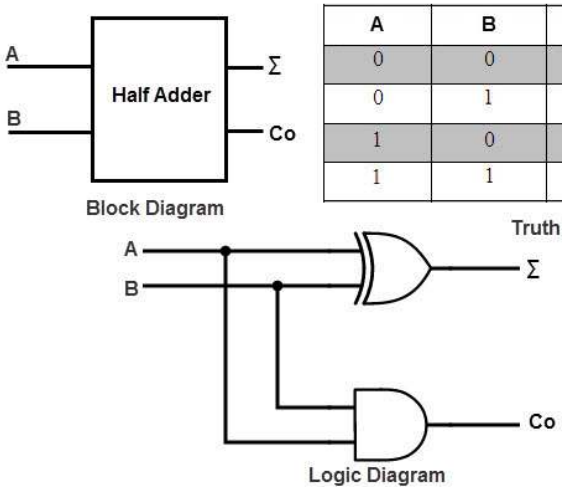
	On supplying the power to the oscillator, the amplitude of the oscillations in the circuit increases until a point is reached wherein the nonlinearities in the amplifier reduce the loop gain to unity.			
IV	Diagram  The Bistable Multivibrator circuit above is stable in both states. Operation Lets suppose that the switch is in the left position, position "A". The base of transistor TR1 will be grounded and in its cut-off region producing an output at Q. That would mean that transistor TR2 is "ON" as its base is connected to Vcc through the series combination of resistors R1 and R2. As transistor TR2 is "ON" there will be zero output at Q, the opposite or inverse of Q. If the switch is now move to the right, position "B", transistor TR2 will switch "OFF" and transistor TR1 will switch "ON" through the combination of resistors R3 and R4 resulting in an output at Q and zero output at Q the reverse of above. Then we can say that one stable state exists when transistor TR1 is "ON" and TR2 is "OFF", switch position "A", and another stable state exists when transistor TR1 is "OFF" and TR2 is "ON", switch position "B".	3 4	7	7

V	 $i = \frac{Vin - Vout}{Rin + Rf}$ therefore, $i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$ $i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$ so, $\frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$ and as, $i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf}$ $\frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$ the Closed Loop Gain (Av) is given as, $\frac{Vout}{Vin} = -\frac{Rf}{Rin}$ Then, the **Closed-Loop Voltage Gain** of an Inverting Amplifier is given as. $Gain\,(Av) = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$ $Vout = -\frac{Rf}{Rin} \times Vin$	3 4		
VI	Diagram  ideal op amp will provide infinite voltage gain	4 3	7	7

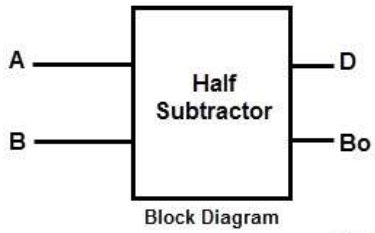
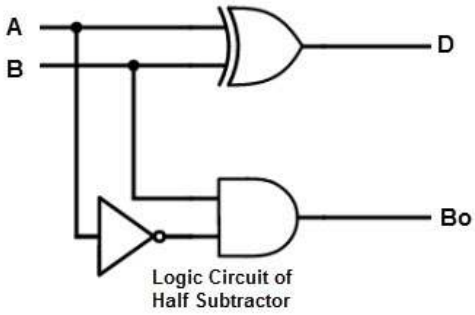
	Gain = Vo/Vin As gain is infinite, Vin = 0 Vin = V2 – V1 In the above circuit V1 is connected to ground, so V1 = 0. Thus V2 (voltage at -ve terminal) also will be at ground potential. V2 = 0			
VII	 Steps Final result	4 3	7	7
VIII	Student must draw symbol and truthtable 	1x7	7	7

IX	 K map Steps Final result (other variations may accept)	4 2 1	7	7
X	**Addition using 2's complement** Initially find the 2's complement of the given negative number. Sum up with the given positive number. If we get the end-around carry 1 then the number will be a positive number and the carry bit will be discarded and remaining bits are the final result. Any one example **Subtraction using 2's complement** In the first step, find the 2's complement of the subtrahend. Add the complement number with the minuend. If we get the carry by adding both the numbers, then we discard this carry and the result is positive else take 2's complement of the result which will be negative. Any one example	1.5 2 1.5 2	7	7
XI	Diagram Explanation  As its name implies, the “ladder” description comes from the ladder-like configuration of the resistors used within the network. A R-2R resistive ladder network provides a simple means of converting digital voltage signals into an equivalent analogue output. Input voltages are applied to the ladder network at various	4 3	7	7

	points along its length and the more input points the better the resolution of the R-2R ladder. The output signal as a result of all these input voltage points is taken from the end of the ladder which is used to drive the inverting input of an operational amplifier			
XII	Diagram Explanation  The **SR flip-flop**, also known as a *SR Latch*, can be considered as one of the most basic sequential logic circuits possible. This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which will "SET" the device (meaning the output = "1"), and is labelled **S** and one which will "RESET" the device (meaning the output = "0"), labelled **R**. The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level "1". Due to this additional clocked input, a JK flip-flop has four possible input combinations, "logic 1", "logic 0", "no change" and "toggle".	4 3	7	7

XIII	 Circuit Operation At the start, the counter is cleared to 0 As the counter counts up with each clock pulse, the Digital to Analog Converter (DAC) outputs a slightly higher voltage. This voltage is compared to the input voltage by the comparator. If the input voltage is greater than the DAC output, the comparator's output will be high and the counter will continue counting normally. Eventually, though, the DAC output will exceed the input voltage, causing the comparator's output to go low. This will be the end of conversion and counter output is the ADC output.	4 3	7	7
XIV	 Truth Table	3.5	7	7

A	B	Sum (∑)	Carry Out (Co)
0	0	**0**	**0**
0	1	**1**	**0**
1	0	**1**	**0**
1	1	**0**	**1**

	 Block Diagram  Logic Circuit of Half Subtractor	A | B | D | B_o 0 | 0 | 0 | 0 0 | 1 | 1 | 1 1 | 0 | 1 | 0 1 | 1 | 0 | 0 Truth Table	3.5		

Module wise question analysis

Question No	Module				No of questions
	I	II	III	IV	
Part A (1 Mark)	2	2	3	2	9
Part B (3 Marks)	4	4	1	1	10
Part C (7 Marks)	2	2	4	4	12
Total questions	**8**	**8**	**8**	**7**	**31**
Total (Marks)=123	**28**	**28**	**34**	**33**	

Cognitive level wise question analysis

Question No	Cognitive level			No of questions
	Remember	Understand	Apply	
Part A (1 Mark)	7	1	1	9
Part B (3 Marks)	5	4	1	10
Part C (7 Marks)	2	7	3	12
Total questions	**14**	**12**	**5**	**31**
Total (Marks)=123	**36**	**62**	**25**	

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